ABSTRACT OF THE DISCLOSURE

A semiconductor memory device is comprised of a plurality of sense amplifiers. The sense amplifiers are arranged in two amplifier columns. The two amplifier columns are disposed between two cell columns of cell plates. An address circuitry, an ATD circuitry, and a delay circuitry are disposed between an input pin row and the two cell columns. An ATD pulse synthesizer is disposed between the two amplifier columns and spaced a predetermined signal transmission path from the ATD and delay circuitries.